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METRIC

Standard Guide for Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Failure Due to Electromigration [Metric] [1]

This standard is issued under the fixed designation F 1259M; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ϵ) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This guide covers recommended design features for test structures used in accelerated stress tests, as described in Test Method F 1260M, to characterize the failure distribution of interconnect metallizations that fail due to electromigration.

1.2 This guide is restricted to structures with a straight test line on a flat surface that are used to detect failures due to an open-circuit or a percent-increase in resistance of the test line.

1.3 This guide is not intended for testing metal lines whose widths are approximately equal to or less than the estimated mean size of the metal grains in the metallization line.

1.4 This guide is not intended for test structures used to detect random defects in a metallization line.

1.5 Metallizations tested and characterized are those that are used in microelectronic circuits and devices.

2. Referenced Documents

2.1 *ASTM Standards:*

F 1260M Test Method for Estimating Electromigration Median-Time-To-Failure and Sigma of Integrated Circuit Metallizations [Metric] [2]

F 1261M Test Method for Determining the Average Electrical Width of a Straight, Thin-Film Metal Line [Metric] [2]

3. Terminology

3.1 *Definitions of Terms Specific to This Standard:*

3.1.1 *test chip*—an area on a semiconductor wafer containing one or more test structures having a specified or implied purpose.

3.1.2 *test structure*—a passive metallization structure, with terminals to permit electrical access that is fabricated on a semiconductor wafer by the normal procedures used to manufacture microelectronic integrated devices.

3.1.3 *metallization*—the thin-film metallic conductor that serves as the primary conductor path in electrical interconnects of microelectronic integrated circuits.

4. Significance and Use

4.1 This guide is intended for the design of test structures used in measuring the median-time-to-failure and sigma (see Test Method F 1260M) of metallizations fabricated in ways that are of interest to the parties to the test.

4.2 This guide is intended to provide design features that facilitate accurate test-line resistance measurements used in estimating metallization temperature. The design features are also intended to promote temperature uniformity along the test line and a minimum temperature gradient at the ends of the test line when significant joule heating is produced during the accelerated stress test.

5. Design Features

5.1 The test structure shall have at least four terminals: two to conduct current and two to measure the voltage. The basic features are illustrated in Fig. 1.

5.1.1 The metallization to be characterized by the test structure shall be in the form of a straight test line of width w, where w shall be larger than the estimated mean size of the metal grains in the metallization of the test line.

NOTE 1—The median-time-to-failure, t_{50}, (see Test Method F 1260M) will be a monotonically increasing function of line width w, when w is larger than the mean size of the metal grains in the test line.

NOTE 2—If the mean size of the metal grains in the test line is larger than the line width, there is an increasing probability, for decreasing line width, that failure will occur in the wider end segment of the structure, rather in the test line, for decreasing line width. This is because both t_{50} and sigma increase with decreasing line width in this regime.

5.1.2 The length of the test line shall be 800 µm. Adjacent-running lines may be included in the design to simulate actual-circuit layout, or to serve as monitor lines to detect electromigration-induced metal extrusions from the test line.

NOTE 3—The specification on the length of the test line is two-fold: to facilitate comparison of t_{50} values (see Test Method F 1260M), because t_{50}

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[2] *Annual Book of ASTM Standards*, Vol 10.04.

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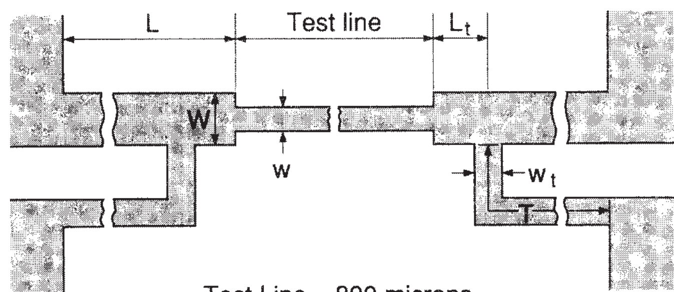

FIG. 1 Design Features of the Electromigration Test Structure

decreases gradually with increasing line length, and to avoid a relatively nonuniform temperature along much shorter test lines when the current-density stress levels are great enough to produce significant joule heating. [3]

NOTE 4—All dimensions specified here and elsewhere are designed dimensions. It is expected that the actual dimensions will differ somewhat due to processing.

5.1.3 Each end of the test line is contacted to a wider line of width $W = 2w$ that extends a distance L to a contact pad or other wide path for conducting the current to and from the test line. The length L shall be longer than approximately 80 µm.

NOTE 5—The purposes of the specifications on the width and length of the end segment are to minimize the temperature gradient at the ends of the test line caused by the heat-sinking effect of the end-segment lines, and to reduce the reservoir of metal available to migrate into the test line. Such a reservoir tends to increase the value of t_{50}.

5.1.4 Each end-contact line shall have a voltage-tap line for measuring voltage. The width of the tap line shall be minimized but shall be no smaller than 1.2 times the minimum resolvable line width. The edge of the tap line shall be adjacent to the end of the end segment, as shown in Fig. 1. The length of each tap line shall be greater than approximately 40 µm.

NOTE 6—The specifications for the length and width of the tap line are for the purposes of reducing the heat-sinking effect of the tap line and the metal available to move into the current path and migrate to the test line.

5.2 Test lines of adjacent electromigration test structures on a single semiconductor chip shall be separated from each other by a distance greater than five times the thickness of the underlying electrical insulator on the semiconductor substrate.

NOTE 7—The specification for separation is for the purpose of minimizing thermal heat transfer between adjacent lines through the underlying oxide.

5.3 A special test structure (see Test Method F 1261M) for measuring the sheet resistance and width of the test line shall be on the same test chip as the electromigration test structure. The test line of the structure shall be parallel to the test line of the electromigration structure and have the same local design features as the test line that can affect the width of the line during fabrication.

6. Keywords

6.1 design guideline; electromigration; electromigration failure; interconnect metallization; metallization open-circuit; metallization resistance; microelectronic; test structure

[3] Schafft, H. A., Staton, T. C., Mandel, J., and Shott, J. D.,“ Reproducibility of Electromigration Measurements,” *IEEE Transactions in Electron Devices*, Vol ED-34, 1987, pp. 673–681.

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