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AMERICAN SOCIETY FOR TESTING AND MATERIALS
100 Barr Harbor Dr., West Conshohocken, PA 19428
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Standard Guide for Analysis of Crystallographic Perfection of Silicon Wafers[1]

This standard is issued under the fixed designation F 1726; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ϵ) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This guide covers the determination of the density of crystallographic defects in unpatterned polished and epitaxial silicon wafers. Epitaxial silicon wafers may exhibit dislocations, hillocks, shallow pits or epitaxial stacking faults, while polished wafers may exhibit several forms of crystallographic defects or surface damage. Use of this practice is based upon the application of several referenced standards in a prescribed sequence to reveal and count microscopic defects or structures.

1.2 Materials for which this practice is applicable may be defined by the limitations of the referenced documents.

1.2.1 This practice is suitable for use with epitaxial or polished wafers grown in either [111] or [100] direction and doped either *p* or *n*-type with resistivity greater than 0.005 Ω-cm.

1.2.2 This practice is suitable for use with epitaxial wafers with layer thickness greater than 0.5 µm.

1.3 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

D 5127 Guide for Electronic Grade Water[2]

F 95 Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer[3]

F 523 Practice for Unaided Visual Inspection of Polished Silicon Wafers Surfaces[3]

F 1241 Terminology of Silicon Technology[3]

F 1809 Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon[3]

F 1810 Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers[3]

2.2 *SEMI Specifications:*

SEMI C-1 Specification for Reagents[4]

3. Terminology

3.1 Defect-related terminology may be found in Terminology F 1241.

4. Summary of Guide

4.1 Clean, unprocessed polished or epitaxial wafers are selected. The wafers are examined under bright light illumination to ensure the sample is free from contamination and obvious surface damage. Epitaxial wafers may also be microscopically inspected before etching to count and classify visible imperfections. Wafers are then etched in a preferential defect etchant solution. The etched surface is again examined under bright light illumination to identify patterns that may be related to contamination or improper handling. The imperfections highlighted by the preferential etchant are then microscopically counted and classified.

5. Significance and Use

5.1 The use of silicon crystals in many semiconductor devices requires a consistent atomic lattice structure. Crystal defects disturb local lattice energy conditions that are the basis for semiconductor behavior. These defects have distinct effects on essential semiconductor-device manufacturing processes such as alloying and diffusion.

5.2 Epitaxial growth processes are used extensively in the manufacture of silicon electronic devices. Stacking faults introduced during epitaxial growth can cause “soft” electrical characteristics and preferential micro plasma breakdowns in diodes.

5.3 Epitaxial defects are more clearly delineated with the use of this destructive etching procedure. Epitaxial wafers may however be classified nondestructively by this method without the destructive preferential etching and inspection steps.

5.4 This guide along with the referenced standards may be used for process control, research and development, and material acceptance purposes.

6. Apparatus

6.1 *Safety Equipment and Facility*, for defect etching are described in Guide F 1809.

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[1] This guide is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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[2] *Annual Book of ASTM Standards*, Vol 11.01.

[3] *Annual Book of ASTM Standards*, Vol 10.05.

[4] Available from Semiconductor Equipment and Materials International, 805 E Middlefield Rd., Mountain View, CA 94043.

6.2 *Wafer Inspection Facilities and Handling Equipment*, shall be consistent with industry practice and suitable for use with Practice F 523.

7. Reagents and Materials

7.1 All chemicals for which such specifications exist shall conform to SEMI Specifications C-1.

7.2 Reference to water shall be understood to mean either distilled water or deionized water, meeting the requirements of Type I water as defined by Guide D 5127.

8. Procedure

8.1 Select an unprocessed, polished or epitaxial wafer, ready for use in the fabrication of electronic devices.

8.1.1 Open the wafer container in a particle controlled environment.

8.1.2 Transfer the wafer with a robotic tool or a nonmetallic vacuum pencil, contacting the wafer edge or backside. Ensure that the front of the adjacent wafer is not contacted during the removal. Any contact with the wafer front can transfer contamination and generally scratch the surface.

8.2 *Preliminary Sample Inspection:*

8.2.1 Inspect the first sample using high intensity light conditions as described in Practice F 523. This macroscopic inspection is intended to identify any surface imperfections, scratches, or contamination hazes that may interfere with the etching process or confound the result. These interferences can generate artifacts that may be confused with the true defects. If any of these interferences are detected, select a separate sample for analysis.

8.2.2 *Epitaxial Wafer, Nondestructive Defect Counting:* Epitaxial wafers may be inspected microscopically before defect etching to count most of the epitaxial stacking fault defects. Epitaxial defects are more clearly delineated with etching, but that is a destructive process. The density of defects is established microscopically, using Test Method F 1810.

8.3 *Defect Etching:* Crystal defects become more clearly visible for unaided eye inspection with increased removal, but resolution of the epitaxial induced defects is reduced with increasing etch times. Refer to Guide F 1809 for more etching information.

8.3.1 *Epitaxial Wafers*—Etch samples with epitaxial layers greater than 2-µm thickness (as measured by Test Method F 95) with removal of at least 0.5 µm to highlight the crystal defects for quantification. Etch samples with epitaxial layers less than 2 µm with removal of no more than 50 % of the layer thickness. Other removal amounts are acceptable based upon producer-consumer agreement.

8.3.2 *Polished Wafers*—The sample must be etched with a removal of 5 to 15 µm to highlight the crystal defects for quantification. Other removal amounts are acceptable based upon producer/consumer agreement.

8.4 *Sample Inspection:* Evaluation of the preferentially etched sample is done in two stages, macroscopic and microscopic.

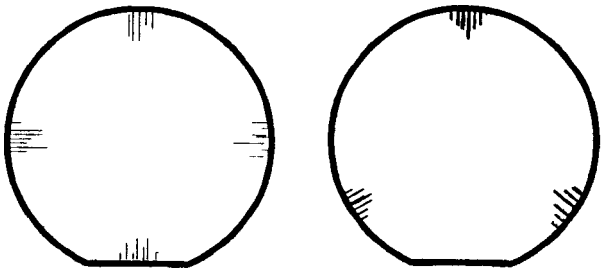
8.4.1 The sample is first inspected using high intensity light conditions as described in Practice F 523. In this macroscopic inspection, patterns of defects are detected. Examples of slip patterns are found in Fig. 1.

8.4.2 A second sample should be obtained if evidence of mechanically or operator induced damage or contamination is observed. These artifacts will interfere with the identification of crystal growth defects. Slip defects may be differentiated from these other observations by insuring that all of the defects are aligned as shown in Fig. 1. Fig. 2 shows the characteristics of scratches or mechanical damage when viewed in high intensity light conditions.

8.5 *Microscopic Defect Counting:* Count and report the density of observed defects using Test Method F 1810.

9. Keywords

9.1 dislocation; epitaxy; grain boundaries; hillock; polycrystalline imperfections; preferential etch; shallow pit; silicon; slip; stacking fault



NOTE 1—The orientation of the wafer defines the locations and direction of the line defects.

FIG. 1 Slip Defects as Seen With Macroscopic High-Intensity Light Inspection

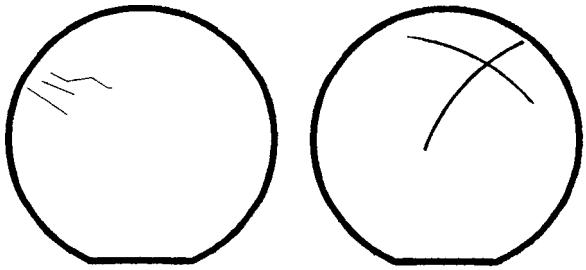


Figure 2a Figure 2b

NOTE 1—The orientation of the wafer does not define the locations and direction of the line defects.

FIG. 2 Typical Scratches (*a*) or Mechanically Induced Defects (b) as Seen With High-Intensity Light Inspection