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AMERICAN SOCIETY FOR TESTING AND MATERIALS
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Standard Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers[1]

This standard is issued under the fixed designation F 1727; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This practice covers the detection of crystalline defects in the surface region of silicon wafers. The defects are induced or enhanced by oxidation cycles encountered in normal device processing. An atmospheric pressure, oxidation cycle representative of bipolar, metal-oxide-silicon (MOS) and CMOS technologies is included. This practice is required to reveal strain fields arising from the presence of precipitates, oxidation induced stacking faults, and shallow etch pits. Slip is also revealed that arises when internal or edge stresses are applied to the wafer.

1.2 Application of this practice is limited to specimens that have been chemical or chemical/mechanical polished to remove surface damage from at least one side of the specimen. This practice may also be applied to detection of defects in epitaxial layers.

1.3 The surface of the specimen opposite the surface to be investigated may be damaged deliberately or otherwise treated for gettering purposes or chemically etched to remove damage.

1.4 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*
D 5127 Guide for Electronic Grade Water[2]
F 1241 Terminology of Silicon Technology[3]
F 1725 Guide for Analysis of Crystallographic Perfection of Silicon Ingots[3]
F 1726 Guide for Analysis of Crystallographic Perfection of Silicon Wafers[3]
F 1809 Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon[3]
F 1810 Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers[3]

2.2 *SEMI Specifications:*[4]
SEMI C-1 Specification for Reagents
SEMI C-3 Specifications for Gases

3. Terminology

3.1 Defect-related terminology may be found in Terminology F 1241.

4. Summary of Practice

4.1 Wet oxidation is used to generate or highlight defects, or both, in silicon wafers. This oxidation may also simulate simple device production processes. The defects are revealed subsequently by preferential etching and examination by interference contrast microscopy according to referenced ASTM standards.

5. Significance and Use

5.1 Defects induced by thermal processing of silicon wafers may adversely influence device performance and yield.

5.2 These defects are influenced directly by contamination, ambient atmosphere, temperature, time at temperature, and rate of change of temperature to which the specimens are subjected. Conditions vary significantly among device manufacturing technologies. The thermal cycling procedures of this practice are intended to simulate basic device processing technologies. Oxidation cycles other than specified herein, or multiple oxidation cycles, may sometimes more accurately simulate device processing procedures. The results obtained may differ significantly from those obtained with the specified oxidation cycles.

5.3 The geometry of some patterns revealed by this practice suggests that they are related to the crystal growth process while others seem related to surface preparation or thermal cycling conditions.

5.4 This practice is suitable for acceptance testing when used with referenced practices and methods.

6. Interferences

6.1 Material having residual work damage in the polished surface exhibits visible patterns when the procedures of this practice are used. Usually, edge damage, lapping damage, tool

[1] This practice is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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[2] *Annual Book of ASTM Standards*, Vol 11.01.

[3] *Annual Book of ASTM Standards*, Vol 10.05.

[4] Available from Semiconductor Equipment and Materials International, 805 E Middlefield Rd., Mountain View, CA 94043.

marks, or scratches are easily identified by the location and pattern observed.

6.2 Contamination not removed by preparatory cleaning procedures or deposited following cleaning, may become visible after oxidation and preferential etching.

6.3 Slip may be introduced by differential expansion at the points of wafer support in the furnace boat. Slip radiating from the points of support may be assumed to originate from this boat pinch and not be inherent in the unprocessed wafer. Slip may also be caused by large thermal gradients imposed across a wafer by fast insertion or removal from the furnace.

6.4 If the oxidation furnace or apparatus is contaminated, it can cause extraneous artifacts or defects.

6.5 Striations, helical features on the surface of a silicon wafer, are ascribed to periodic dopant incorporation differences occurring at the rotating solid-liquid interface during crystal growth. These features are visible to the unaided eye after preferential etching, seem continuous under 100× magnification, and may be confused with ring patterns of oxidation stacking faults.

6.6 Otherwise identical wafers with different back surface conditions may yield different results by this practice.

6.7 Wafers, particularly <111> orientation, may show lower shallow-pit defect density when the back surface of the wafer is gettered. Backside gettering should be noted in the sample classification when data are reported.

7. Apparatus

7.1 *Oxidation Furnace*—furnace shall be consistent with the intended process application and shall sustain a designated temperature with uniformity less than ± 5°C over a zone at least 0.3-m long.

7.2 *Steam Source*—wet oxidation shall be carried out using a pyrogenic steam generator to provide steam.

7.3 *Working Chamber*—a pure, fused quartz, silicon carbide, or silicon tube of an inside diameter sufficient to hold the specimen wafers. The inlet end shall be fitted with the appropriate pyrogenic torch apparatus. The exhaust end shall be fitted to exhaust the process gases to satisfy applicable environmental requirements and prevent back streaming of outside air into the working chamber.

7.4 *Wafer Boat*—a quartz, silicon or silicon carbide fixture for holding the specimen wafers either parallel or perpendicular to the gas flow in the furnace.

7.5 *Pickup Tool*—a manual or automated transfer tool fitted with a nonmetallic material such as quartz or TFE-fluorocarbon. The pickup tool shall be constructed so that no metal can contact the specimen wafer.

8. Reagents and Materials

8.1 *Purity and Concentration of Reagents*—Chemicals shall conform to SEMI Specifications C-1 where they exist. Gases shall conform to SEMI Specifications C-3.

8.2 *Purity of Water*—Reference to water shall be understood to mean either distilled water or deionized water, meeting the requirements of Type I water as defined by Guide D 5127.

9. Hazards

9.1 When removed from the oxidation furnace, silicon wafers and quartz accessories are extremely hot. Take care to allow the materials adequate time to cool before handling.

9.2 Pyrogenic steam oxidation uses heated hydrogen and oxygen to grow a wet oxide layer. Improper or uncontrolled combination of these gases can result in fire or explosion.

9.3 Hydrofluoric acid solutions are particularly hazardous and the specific preventive measures must be strictly observed.

9.4 Safety or protective gear should be worn while handling acid solutions. Safety requirements vary, but the essentials are: plastic gloves, safety glasses, face shield, acid gown, and shoe covers.

10. Sampling

10.1 Select specimens to represent the lot to be tested as specified in producer/consumer agreements.

11. Specimen Preparation

11.1 Commonly this practice may be used for wafers as they are received; however, the parties using this practice may establish a uniform cleaning procedure before oxidation.

12. Preparation of Apparatus

12.1 The oxidation furnace tube (working chamber) and associated quartzware shall be maintained in a state suitable for producing oxides appropriate for the process for which the wafers are being tested.

12.2 Immediately before use, clean the pickup tool using standard industry practices.

13. Procedure

13.1 Handle wafers only with a clean, nonmetallic pickup tool or automated transfer unit to avoid scratching or contaminating the surface.

13.2 Oxidize the wafers by the procedure in Table 1 or by a procedure acceptable to both producer and consumer.

13.2.1 Preheat the furnace to the push temperature.

13.2.2 Load the specimen wafers into the wafer boat, being careful to avoid binding, scratching, or contamination.

13.2.3 Insert the boat into the hot zone at the rate called for in Table 1. The wafer boat shall be centered in the uniform hot zone.

TABLE 1 Oxidation Procedure

Step	Function	Conditions
1. Push (Load)	Ambient	Dry Oxygen
	Temperature	800°C
	Push Rate	200 mm/minute
2. Temperature Ramp	Ambient	Dry Oxygen
	Temperature Ramp	+5°C/minute
	Final Temperature	1100°C
3. Oxidation	Ambient	Steam (wet oxide)
	Temperature	1100°C
	Time	60 minute
4. Temperature Ramp	Ambient	Dry Oxygen
	Temperature Ramp	–3°C/minute
	Final Temperature	800°C
5. Pull (Unload)	Ambient	Dry Oxygen
	Temperature	800°C
	Pull Rate	200 mm/minute

13.2.4 Follow the ramp up, oxidation, ramp down, and pull procedures.

13.3 Transfer the room temperature wafers from the quartz boat to a wafer carrier using the pickup tool or automated transfer unit.

13.4 Remove the thermal oxide layer using hydrofluoric acid, (49 %) for 2 min followed by deionized water rinse and spin dry.

13.5 Select and use an appropriate etching solution to allow defect delineation while removing 4 µm (or another amount as agreed upon between the parties to the test) of silicon from the surface being evaluated.

NOTE 1—Refer to Guide F 1809.

13.6 Count and report the density of observed defects using Test Method F 1810.

14. Keywords

14.1 defects; dislocation; epitaxy; hillock; imperfections; oxidation; preferential etch; shallow pit; silicon; slip; stacking fault; swirl